Course Profile

Course Name:-	**Computer Architecture**
Course Code:-	**CEN 326/CEN211**
Academic Year:-	**1434-1435(H)**
Semester:-	**I**

Course Overview

This Course is designed to develop knowledge and understanding of the principles of computer architecture and provides an opportunity to apply this through the use of contemporary hardware and software. The overall theme of the course is the relationship between design and knowledge, this course aims to familiarize the student with the basics of computer architecture as well as the recent advances of computer architecture, as well as the main elements of a computer system. The focus of the course is to impart in the students useful skills that will enhance their ability to identify computers and its design so as to make better choice Additional goal of the course is to teach the student the design considerations of each component on the computer system. Besides the student will know how instructions are processed and arithmetic are carried, by learning the basics on multiprocessors and clusters.. Topics include History of computers. Basic computer organization,Data representation; Design of a hardwired-controlled basic computer; Processor organization; ALUs, bus and stack organizations; Instruction sets and instruction formats; Machine and Assembly language programming. Assembler function and design, System software, Micro-programmed CPU, Comparison between CISC, RISC and VLIW processors, Introduction to memory organization; I/O operations; Introduction to parallel processing techniques.

Course Details	
Level:-	**5**
Credit:-	**3**
Pre-Requisites:-	CEN 311
Co- Requisites:-	

Learning Outcomes of Course

On successful completion of this course, you will be able to:

1. Understand the concept of Computer Design and factors that contribute to computer performance and Select the most appropriate performance metric when evaluating a computer.
2. Understand the concept of Processor organization, Instruction sets and instruction formats
3. Understand & Demonstrate Machine & Assembly language programming and Assembler function and design
4. Identify the characteristics of CISCS, RISC, and VLIW processors.
5. Analyze the effect of memory on performance and analyze performance of multilevel caches systems.
6. Analyze Input/output systems, multicore, multiprocessors, cluster and new trends in Computer Architecture.

Course Assessment

Name of Assessment Task	Weight of Assessment	Week Due
1. Midterm Exam-1	**20%**	**6**
2. Midterm Exam-2	**20%**	**12**
3. Quizzes	**10%**	**4,9,13**
4. Assignments/Report/Seminar	**10%**	**3,5,8,10,14**
5. Final Exam	**40%**	**16**

Assessment Task and Learning Outcomes Alignment

Assessment Task Name	Course Learning Outcomes					
	1	**2**	**3**	**4**	**5**	**6**
1. Midterm Exam-1	√	√	√			
2. Midterm Exam-2			√	√	√	
3. Quizzes	√	√	√	√	√	√
4. Assignments/Report/Seminar	√	√	√	√	√	√
5. Final Exam	√	√	√	√	√	√

Teaching Contact Details

Course Coordinator:	**Shailendra Mishra, Ph.D**
Lab/Tutorial Instructor:	**Mohammed AbdulKhader, M.S**
Email:	s.mishra@mu.edu.sa a.mohammed@mu.edu.sa
Office Hours:	Thursday 9.00 a.m. to 11.00 a.m.
Office Number:	0164045382
Office:	Level 1, CCIS Building Room No-024-1-20-3

Details of Required Text Book

Book Name	**Authors Name**	Publisher	**Year**	**Edition**
1.Computer Organization and Design, the hardware/software interface,	Hennessy and Patterson	The Morgan Kaufmann Series in Computer Architecture and Design	2011	5th

Details of Required Reference Books

Book Name	**Authors Name**	**Publisher**	**Year**	**Edition**
1. Computer Organization and Architecture: Designing for Performance	William Stallings	Prentice Hall	2012	9th
2. Computer System Architecture	M.Mano	Prentice Hall	1992	**3rd**

IT Resources

The following IT Resources will require to access-

- http://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-823-computer-system-architecture-fall-2005/lecture-notes/
- http://www.cs.ccsu.edu/~markov/ccsu_courses/385Syllabus.html

Course Schedule

Module/Topic	Chapter	Event and submission	Week
Computer Evolution Basic computer organization	Chapter 2, (Computer Evolution) William Stallings, Computer Organization and Architecture: Designing for Performance, 9th Edition, Prentice Hall, 2012 Chap. 5 (Basic Computer Organization and Design), Computer System Architecture M. Morris Mano,	Brain storming and review of previous knowledge.	Week-1
Data representation; Design of a hardwired-controlled basic computer;	Chap.3,Data representation , Computer System Architecture,M. Morris Mano, Chapter 19,Control Unit Operation, William Stallings, Computer Organization and Architecture: Designing for		Week-2

	Performance, 9th Edition, Prentice Hall, 2012		
Processor organization; ALUs, bus and stack organizations	Chap. 8 Central Processing Unit General register organization, the operation of memory stack, Computer System Architecture, M. Morris Mano,	Assignment I	Week-3
Instruction sets and instruction formats	Chapter 4, Hennessy and Patterson, Computer Organization and Design, the hardware/software interface, 5th Edition. Chapter 12,13 William Stallings, Computer Organization and Architecture: Designing for Performance, 9th Edition, Prentice Hall, 2012	Quiz 1	Week-4
Machine and Assembly language programming.	Chap. 6 Programming the Basic Computer, Computer System Architecture, M. Morris Mano,	Assignment II	Week-5
		Written Assessment Due	Week-6
Assembler function and design.	Appendix B, William Stallings, Computer Organization and Architecture: Designing for Performance, 9th		Week-7

	Edition, Prentice Hall, 2012		
System software. Micro-programmed CPU	Chap. 7, Microprogrammed Control, Computer System Architecture,M. Morris Mano, Chapter 20, Microprogrammed ,Control, William Stallings, Computer Organization and Architecture: Designing for Performance, 9th Edition, Prentice Hall, 2012	Assignment III	Week-8
CISCS, RISC, and VLIW processors	Chapter 15, William Stallings, Computer Organization and Architecture: Designing for Performance, 9th Edition, Prentice Hall, 2012	Quiz II	Week-9
Introduction to memory organization(Memory Hierarchy, Virtual memory)	Chapter 5, Hennessy and Patterson, Computer Organization and Design, the hardware/software interface, 5th Edition.	Assignment IV	Week-10
I/O operations	Chapter 6, Hennessy and Patterson, Computer Organization and hardware/software interface, 5th Edition Design, the.		Week-11

		Written Assessment Due	Week-12
Introduction to parallel processing techniques	Chapter 17, William Stallings, Computer Organization and Architecture: Designing for Performance, 9th Edition, Prentice Hall, 2012	Quiz III	Week-13
New trends in computer architecture((Multicore, multiprocessors, and clusters)	Chapter7, Hennessy and Patterson, Computer Organization and Design, the hardware/software interface, 5th Edition.	Assignment V	Week-14
			Review Exam Week
			Exam Week

The **American Psychological Association (APA)** referencing style must be use for all submissions of this course.

Course Assessment Task

WRITTEN ASSESMENT (Mid Term I Exam)

Assessment Title	Written Assessment
Task Description	This assignment is aligned to learning outcomes 1, 2,3 In that regard, the assignment contains questions that assess: 1. Understand the concept of Computer Design and factors that contribute to computer performance and Select the most appropriate performance metric when evaluating a computer. 2. Understand the concept of Processor organization, Instruction sets and instruction formats 3. Understand & Demonstrate Machine & Assembly language programming
Assessment Due Date	**Week 6**
Return Date to Students	Week 7
Weighting	20%
Assessment Criteria	The assessment criteria for this task are under continuous revision.
Referencing Style	American Psychological Association (APA)
Submission	
Learning Outcomes Assessed	1. Understand the concept of Computer Design and factors that contribute to computer performance and Select the most appropriate performance metric when evaluating a computer. 2. Understand the concept of Processor organization, Instruction sets and instruction formats 3. Understand & Demonstrate Machine & Assembly language programming

WRITTEN ASSESMENT (Mid Term II Exam)

Assessment Title	Written Assessment
Task Description	This assignment is aligned to learning outcomes 3,4, 5, In that regard, the assignment contains questions that assess: • Understand & Demonstrate Assembler function and design • Identify the characteristics of CISCS, RISC, and VLIW processors. • Analyze the effect of memory on performance and analyze performance of multilevel caches systems.
Assessment Due Date	**Week 12**
Return Date to Students	Week 13
Weighting	20%
Assessment Criteria	The assessment criteria for this task are under continuous revision.
Referencing Style	American Psychological Association (APA)
Submission	
Learning Outcomes Assessed	• Understand & Demonstrate Assembler function and design • Identify the characteristics of CISCS, RISC, and VLIW processors. • Analyze the effect of memory on performance and analyze performance of multilevel caches systems

FINAL EXAMINATION

Outline	**Complete an examination**
Date	**During University examination period**
Weighting	**40%**
Length	180 Minutes
Details	Dictionary - non-electronic, concise, direct translation only (dictionary must not contain any notes or comments) No Calculator Permitted Closed Books
Learning Outcomes Assessed	1 Understand the concept of Computer Design and factors that contribute to computer performance and Select the most appropriate performance metric when evaluating a computer. 2 Understand the concept of Processor organization, Instruction sets and instruction formats 3 Understand & Demonstrate Machine & Assembly language programming and Assembler function and design 4 Identify the characteristics of CISCS, RISC, and VLIW processors. 5 Analyze the effect of memory on performance and analyze performance of multilevel caches systems. 6 Analyze Input/output systems , multicore, multiprocessors, cluster and new trends in CA