CEN 326

Computer Architecture

Term 2 - 2014

Course Profile

All details in this course profile for CEN 326 have been officially approved by CCIS Majmaah University and represent a learning partnership between the University and you (our student). The information will not be change unless absolutely necessary and any change will be clearly indicated by an approved correction included in the profile.

General Information

OVERVIEW

This Course is designed to develop knowledge and understanding of the principles of computer architecture and provides an opportunity to apply this through the use of contemporary hardware and software. The overall theme of the course is the relationship between design and knowledge, this course aims to familiarize the student with the basics of computer architecture as well as the recent advances of computer architecture, as well as the main elements of a computer system. The focus of the course is to impart in the students useful skills that will enhance their ability to identify computers and its design so as to make better choice Additional goal of the course is to teach the student the design considerations of each component on the computer system. Besides the student will know how instructions are processed and arithmetic are carried, by learning the basics on multiprocessors and clusters.. Topics include History of computers. Basic computer organization. Data representation; Design of a hardwired-controlled basic computer; Processor organization; ALUs, bus and stack organizations; Instruction sets and instruction formats; Machine and Assembly language programming. Assembler function and design, System software, Micro-programmed CPU, Comparison between CISC, RISC and VLIW processors, Introduction to memory organization; I/O operations; Introduction to parallel processing techniques.

DETAILS

Level	5
Credit Points	3

PRE-REQUISITES OR CO-REQUISITES

Pre-requisite: CEN 311

ATTENDANCE Requirements

All on-campus students are expected to attend scheduled classes – in some courses, these classes axe identified as a mandatory (pass/fail) component and attendance is compulsory.

ASSESSMENT OVERVIEW

Assessment Task	Weighting
1. Midterm Exam-1	15%
2. Midterm Exam-2	15%
3. Quizzes	5%
4. Assignments/Report/Seminar	5%
5. Lab	20%
6. Final Exam	40%

This is a graded course: your overall grade will be calculated from the marks or grades for each assessment task, based on the relative weightings shown in the table above. You must obtain an overall mark for the course of at least 60%, or an overall grade of 'pass' in order to pass the course. If any 'pass/fail' tasks are shown in the table above they must also be completed successfully ('pass' grade). You must also meet any minimum mark requirements specified for a particular assessment task, as detailed in the 'assessment task' section (note that in some instances, the minimum mark for a task may be greater than 50%). Consult the University's Grades and Results Procedures for more details of interim results and final grades.

Majmaah University Policies

All University policies are available on the mu.deu.sa .

You may wish to view these policies:

- Assessment of Coursework Procedures
- Grads and Results Procedure
- Review ox Grade Policy
- Plagiarism Procedure
- Student Misconduct and Plagiarism Policy

- Monitoring Academic Progress Policy
- Monitoring Academic Progress Policy
- Monitoring Academic Progress Procedures
- Refund Excess Payments (Credit Balances) Policy
- Student complaints Policy
- Use of Internet, mail and Computing Facilities Policy

This list is not an exhaustive list of all University policies. The full lists of University policies are available on the University Web site(www.mu.edu.sa)

Course Learning outcomes

On successful completion of this course, you will be able to:

1. Understand the concept of Computer Design and factors that contribute to computer performance and Select the most appropriate performance metric when evaluating a computer.
2. Understand the concept of Processor organization, Instruction sets and instruction formats
3. Understand & Demonstrate Machine & Assembly language programming and Assembler function and design
4. Identify the characteristics of CISCS, RISC, and VLIW processors.
5. Analyze the effect of memory on performance and analyze performance of multilevel caches systems.
6. Analyze Input/output systems , multicore, multiprocessors, cluster and new trends in Computer Architecture.

Learning outcomes, Assessment and Graduate attributes

ALLIGNMENT OF ASSESSMENT TASKS TO LEARNING OUTCOMES

Assessment Task	Learning Outcomes					
	1	2	3	4	5	6
1. Midterm Exam-1	.	.	.			
2. Midterm Exam-2			.	.	.	
3. Quizzes	.	.	.	.	.	.
4. Assignments/Report/Seminar	.	.	.	.	.	.
5. Lab Exam	.	.	.	.	.	.
6. Final Exam	.	.	.	.	.	.

Textbook and Resources

Computer Organization and Design, the hardware/software interface, Hennessy and Patterson

Computer System Architecture, M.Mano. Prentice Hall

Computer Organization and Architecture: Designing for Performance, 9th Edition, Prentice Hall, 2012

PRESCRIBED TEXTBOOKS

Author/s	Hennessy and Patterson	Year	2011
Edition	5th	Publisher	The Morgan Kaufmann Series in Computer Architecture and Design
Author/s	M.Mano	Year	1992
Edition	3rd	Publisher	Prentice Hall
Author/s	: William Stallings	Year	: 2012
Edition	9th	Publisher	Prentice Hall

IT RESOURSES

You will need access to the following IT resources:

- http://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-823-computer-system-architecture-fall-2005/lecture-notes/
- http://www.cs.ccsu.edu/~markov/ccsu_courses/385Syllabus.html

Referencing style

All submissions for this course must use the **American Psychological Association (APA)** referencing style ,For further information, see the Assessment Tasks below.

Teaching Contacts

Course Coordinator	**Prof. Shailendra Mishra** **College of Computer & Information Sciences** **Majmaah University,Majmaah,KSA**

Schedule

Week	Module/Topic	Chapter	Event and submission
Week-1	Computer Evolution Basic computer organization	Chapter 2, (Computer Evolution) William Stallings, Computer Organization and Architecture: Designing for Performance, 9th Edition, Prentice Hall, 2012 Chap. 5 (Basic Computer Organization and Design), Computer System Architecture M. Morris Mano,	Brain storming and review of previous knowledge.
Week-2	Data representation; Design of a hardwired-controlled basic computer;	Chap.3,Data representation , Computer System Architecture,M. Morris Mano, Chapter 19,Control Unit Operation, William Stallings, Computer Organization and	

		Architecture: Designing for Performance, 9th Edition, Prentice Hall, 2012	
Week-3	Processor organization; ALUs, bus and stack organizations	Chap. 8 Central Processing Unit General register organization, the operation of memory stack, Computer System Architecture, M. Morris Mano,	Assignment I
Week-4	Instruction sets and instruction formats	Chapter 4, Hennessy and Patterson, Computer Organization and Design, the hardware/software interface, 5th Edition. Chapter 12,13 William Stallings, Computer Organization and Architecture: Designing for Performance, 9th Edition, Prentice Hall, 2012	Quiz 1
Week-5	Machine and Assembly language programming.	Chap. 6 Programming the Basic Computer, Computer System Architecture, M. Morris Mano,	Assignment II
Vacation week			
Week-6			**Written Assessment Due** **Sunday (16 March 2014) 10:00 PM**

Week-7	Assembler function and design.	Appendix B, William Stallings, Computer Organization and Architecture: Designing for Performance, 9th Edition, Prentice Hall, 2012	
Week-8	System software. Micro-programmed CPU	Chap. 7, Microprogrammed Control, Computer System Architecture,M. Morris Mano, Chapter 20, Microprogrammed ,Control, William Stallings, Computer Organization and Architecture: Designing for Performance, 9th Edition, Prentice Hall, 2012	Assignment III
Week-9	CISCS, RISC, and VLIW processors	Chapter 15, William Stallings, Computer Organization and Architecture: Designing for Performance, 9th Edition, Prentice Hall, 2012	Quiz II
Week-10	Introduction to memory organization(Memory Hierarchy, Virtual memory)	Chapter 5, Hennessy and Patterson, Computer Organization and Design, the hardware/software interface, 5th Edition.	Assignment IV
Week-11			**Written Assessment Due** **Sunday (20 April 2014) 10:00 AM**

Week-12	I/O operations	Chapter 6, Hennessy and Patterson, Computer Organization and Design, the hardware/software interface, 5th Edition.	
Week-13	Introduction to parallel processing techniques	Chapter 17, William Stallings, Computer Organization and Architecture: Designing for Performance, 9th Edition, Prentice Hall, 2012	Quiz III
Week-14	New trends in computer architecture((Multicore, multiprocessors, and clusters)	Chapter7, Hennessy and Patterson, Computer Organization and Design, the hardware/software interface, 5th Edition.	Assignment V
Review Exam Week			
Exam Week			

Teaching Contacts

Contact information

Course Coordinator:	**Shailendra Mishra, Ph.D**
Lab/Tutorial Instructor:	
Email:	s.mishra@mu.edu.sa
Office Hours:	8.00 a.m. to 02.30 p.m.
Office Number:	0164045382
Office:	Level 1, CCIS Building Room No-3-2-20-2, CCIS, Majmaah University

For any individual queries, please email me and I will endeavour to reply as soon as practical.

Assessment Task

WRITTEN ASSESMENT (Mid Term I Exam)

Assessment Title	Written Assessment
Task Description	This assignment is aligned to learning outcomes 1, 2,3 In that regard, the assignment contains questions that assess: 1. Understand the concept of Computer Design and factors that contribute to computer performance and Select the most appropriate performance metric when evaluating a computer. 2. Understand the concept of Processor organization, Instruction sets and instruction formats 3. Understand & Demonstrate Machine & Assembly language programming
Assessment Due Date	**Week 6 Monday (17 March 2014)10 :00 AM**
Return Date to Students	Week 7
Weighting	15%
Assessment Criteria	The assessment criteria for this task are under continuous revision.
Referencing Style	American Psychological Association (APA)
Submission	
Learning Outcomes Assessed	1. Understand the concept of Computer Design and factors that contribute to computer performance and Select the most appropriate performance metric when evaluating a computer. 2. Understand the concept of Processor organization, Instruction sets and instruction formats 3. Understand & Demonstrate Machine & Assembly language programming

WRITTEN ASSESMENT (Mid Term II Exam)

Assessment Title	Written Assessment
Task Description	This assignment is aligned to learning outcomes 3,4, 5, In that regard, the assignment contains questions that assess: • Understand & Demonstrate Assembler function and design • Identify the characteristics of CISCS, RISC, and VLIW processors. • Analyze the effect of memory on performance and analyze performance of multilevel caches systems.
Assessment Due Date	**Week 12**
Return Date to Students	Week 13
Weighting	15%
Assessment Criteria	The assessment criteria for this task are under continuous revision.
Referencing Style	American Psychological Association (APA)
Submission	
Learning Outcomes Assessed	• Understand & Demonstrate Assembler function and design • Identify the characteristics of CISCS, RISC, and VLIW processors. • Analyze the effect of memory on performance and analyze performance of multilevel caches systems

FINAL EXAMINATION

Outline	Complete an examination
Date	**During University examination period**
Weighting	**40%**
Length	180 Minutes
Details	Dictionary - non-electronic, concise, direct translation only (dictionary must not contain any notes or comments) No Calculator Permitted Closed Books
Learning Outcomes Assessed	1 Understand the concept of Computer Design and factors that contribute to computer performance and Select the most appropriate performance metric when evaluating a computer. 2 Understand the concept of Processor organization, Instruction sets and instruction formats 3 Understand & Demonstrate Machine & Assembly language programming and Assembler function and design 4 Identify the characteristics of CISCS, RISC, and VLIW processors. 5 Analyze the effect of memory on performance and analyze performance of multilevel caches systems. 6 Analyze Input/output systems , multicore, multiprocessors, cluster and new trends in CA